JC13 Rec'd PCT/PTO 0 6 APR 2001

FORM PTO-1390 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTORNEY'S DOCKET NO. PHQ 99,010
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		U.S. Application No. (if known, see 37 CFR 1.5) 09/807067
INTERNATIONAL APPLICATION NO. PCT/EP00/07519	INTERNATIONAL FILING DATE August 2, 2000	PRIORITY DATE CLAIMED August 9, 1999

TITLE OF INVENTION
METHOD OF MANUFACTURING AN INTEGRATED CIRCUIT COMPRISING AN IMPROVED SILICIDATION AND A CORRESPONDING INTEGRATED CIRCUIT

APPLICANT(S) FOR DO/EO/US
WALTER JAN AUGUST DE COSTER, ERIC GERRITSEN and MARIE-THERESE BASSO

Applicant(s) herewith submit to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [X] This is a FIRST submission of items concerning a filing under 35 U.S.C. 371.

2. [ ] This is a SECOND or SUBSEQUENT submission of items concerning a filing under 35 U.S.C. 371.

3. [X] This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).

4. [ ] A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.

5. [X] A copy of the International Application as filed (35 U.S.C. 371 (c)(2))
   a. [X] is transmitted herewith (required only if not transmitted by the International Bureau).
   b. [ ] has been transmitted by the International Bureau.
   c. [ ] is not required, as the application was filed in the United States Receiving Office (RO/US).

6. [ ] A translation of the International Application into English (35 U.S.C. 371(c)(2))

7. [X] Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. [ ] are transmitted herewith (required only if not transmitted by the International Bureau).
   b. [ ] have been transmitted by the International Bureau.
   c. [ ] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [X] have not been made and will not be made.

8. [ ] A translation of the amendment to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)).

9. [X] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).

10. [ ] A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. To 16. Below concern document(s) or information included:

11. [ ] An Information Disclosure Statement under 37 C.F.R. 1.97 and 1.98.

12. [X] An assignment document for recording. A separate cover sheet is compliance with 37 C.F.R. 3.28 and 3.31 is included.

13. [X] A FIRST preliminary amendment.
    [ ] A SECOND OR SUBSEQUENT preliminary amendment.

14. [ ] A substitute specification.

15. [X] A change of power of attorney and/or address letter.

16. [X] Other items or information:
    8 Sheets of formal drawing
    Authorization under 37 CFR 1.136 (a) (3)

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DATE OF DEPOSIT April 6, 2001

I HEREBY CERTIFY THAT THIS PAPER OR FEE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE "EXPRESS MAIL POST OFFICE TO ADDRESSEE" SERVICE UNDER 37 CFR 1.10 ON THE DATE INDICATED ABOVE AND IS ADDRESSED TO THE COMMISSIONER OF PATENTS AND TRADEMARKS, WASHINGTON, D.C. 20231.

Patti DeMichele

(TYPED OR PRINTED NAME OF PERSON MAILING PAPER OR FEE)

(SIGNATURE OF PERSON MAILING PAPER OR FEE)

U.S. APPLICATION NO. (If known, see 37 C.F.R. 1.5) 09/807067	INTERNATIONAL APPLICATION NO. PCT/EP00/07519	ATTORNEY'S DOCKET NUMBER PHQ 99,010

17 [X] The following fees are submitted:

BASIC NATIONAL FEE (37 C.F.R. 1.492(A)(1)-(5)):

		CALCULATIONS (PTO USE ONLY)
Search Report has been prepared by the EPO or JPO	$ 690.00	
International preliminary-examination fee paid to USPTO (37 C.F.R. 1.482)	$ 710.00	
No international preliminary examination fee paid to USPTO (37 C.F.R. 1.482) but international search fee paid to USPTO (37 C.F.R. 1.445(a)(2)	$1000.00	
Neither international preliminary examination fee (37 C.F.R. 1.482) nor international search fee (37 C.F.R. 1.445(a)(2)) paid to USPTO	$ 100.00	
International preliminary examination fee paid to USPTO (37 C.F.R. 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4)	$ 860.00	
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 690.00	$

Surcharge of $130.00 for furnishing the oath or declaration later than [ ] 20 [ ] 30 months from the earliest claimed priority date (37 C.F.R. 1.492(e)).	$	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total Claims	9 - 20 =		X $ 18.00	$	
Independent claims	2 - 3 =		X $ 80.00	$	
MULTIPLE DEPENDENT CLAIMS (if applicable)			+ $270.00	$	
TOTAL OF ABOVE CALCULATIONS			=	$ 690.00	
Reductions by 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 C.F.R. 1.9, 1.27, 1.28)				$	
SUBTOTAL			=	$ 690.00	
Processing fee of $130.00 for furnishing the English translation later than [ ] 20 [ ] 30 months from the earliest claimed priority date (37 C.F.R. 1.492(f)).			+	$	
TOTAL NATIONAL FEE			=	$ 690.00	
Fee for recording the enclosed assignment (37 C.F.R. 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 C.F.R. 3.28,3.31). $40.00 per property			+	$ 40.00	
TOTAL FEES ENCLOSED			=	$	
				Amount to be Refunded	$
				Charged	$ 980.00

a. [ ] A check in the amount $_____ to cover the above fees is enclosed.

b. [X] Please charge my Deposit Account No. 14-1270 in the amount of $730.00 to cover the above fees. A duplicate copy of this sheet is enclosed.

c. [X] The Commissioner is hereby authorized to charge any additional fee, with the exception of the Base Issue Fee, which may be required, or credit any overpayment to Deposit Account No. 14-1270. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 C.F.R. 1.494 or 1.495 has not been met, a petition to revive (37 C.F.R. 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Corporate Patent Counsel
Philips Electronics North America Corporation
580 White Plains Road
Tarrytown, NY 10591

DATE OF MAILING: April 6, 2001

(SIGNATURE)

STEVEN R. BIREN
(NAME)

26,531
(REGISTRATION NUMBER)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

WALTER J.A. DE COSTER ET AL

Atty. Docket

PHQ 99,010

Serial No.

Filed: CONCURRENTLY

METHOD OF MANUFACTURING AN INTEGRATED CIRCUIT COMPRISING AN IMPROVED SILICIDATION AND A CORRESPONDING INTEGRATED CIRCUIT

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to calculation of the filing fee and examination, please amend the above-identified application as follows:

IN THE CLAIMS

Please amend the claims as follows:

3. (Amended) A method as claimed in claim 1, characterized in that the depth (h) of the trench is equal to maximally half the height (H1) of the larger isolation layer and maximally half the thickness (E) of the larger isolation layer.

4. (Amended) A method as claimed in claim 1, characterized in that
the vertical portion of the smaller isolation layer (402) is anisotropically etched.

5. (Amended) A method as claimed in claim 1, characterized in that the vertical portion of the smaller isolation layer (402) is isotropically etched.

8. (Amended) An integrated circuit as claimed in claim 6, characterized in that the depth (h) of the trench (TR) is equal to maximally half the height (H1) of the larger isolation layer and equal to maximally half the thickness(E) of the larger isolation layer.

9. (Amended) An integrated circuit as claimed in claim 6, characterized in that each lateral isolation region comprises a horizontal trench (TH) made in the smaller isolation layer (402) between the larger isolation layer (411) and the substrate (1) of the integrated circuit, said trench extending from the lateral edge of the larger isolation layer of the lateral isolation region.

REMARKS

The claims have been amended in order to reformat the claims to delete all multiple dependencies prior to calculation of the filing fee and place the instant application in standard U.S. format.

Entry of this amendment prior to calculating the filing fee is respectfully requested.

Respectfully submitted,

By _____
Steven R. Biren, Reg. 26,531
Attorney
(914) 333-9630
April 6, 2001

APPENDIX

3. (Amended) A method as claimed in claim 1 ~~or 2~~, characterized in that the depth (h) of the trench is equal to maximally half the height (H1) of the larger isolation layer and maximally half the thickness (E) of the larger isolation layer.

4. (Amended) A method as claimed in claim 1 ~~any one of the preceding claims~~, characterized in that the vertical portion of the smaller isolation layer (402) is anisotropically etched.

5. (Amended) A method as claimed in claim 1 ~~any one of the claims 1 to 3~~, characterized in that the vertical portion of the smaller isolation layer (402) is isotropically etched.

8. (Amended) An integrated circuit as claimed in claim 6 ~~or 7~~, characterized in that the depth (h) of the trench (TR) is equal to maximally half the height (H1) of the larger isolation layer and equal to maximally half the thickness(E) of the larger isolation layer.

9. (Amended) An integrated circuit as claimed in claim 6 ~~any one of the claims 6 to 8~~, characterized in that each lateral isolation region comprises a horizontal trench (TH) made in the smaller isolation layer (402) between the larger isolation layer (411) and the substrate (1) of the integrated circuit, said trench extending from the lateral edge of the larger isolation layer of the lateral isolation region.

Method of manufacturing an integrated circuit comprising an improved silicidation and a corresponding integrated circuit

The invention relates to the manufacture of an integrated circuit, more particularly to the formation of metal silicide zones on the polysilicon regions forming, for example, the gate regions of the field effect transistors.

In Figure 1, which very diagrammatically shows a field effect transistor in accordance with the prior art the gate of which is covered with a metal silicide 5, reference numeral 1 denotes a semiconductor substrate within which the field effect transistor is formed. As is customary, said field effect transistor comprises a projecting portion of polysilicon 2, which forms the gate region of the transistor, said projecting portion being isolated from the substrate by a gate oxide 3, which typically consists of silicon dioxide.

The transistor also comprises lateral isolation zones or spacers 4, which are provided at the sides of the gate region 2 so as to be in contact therewith. These spacers are customarily composed of two layers, i.e. a smaller isolation layer 40, which is generally composed of an oxide (for example, tetraethyl orthosilicate (Si $(OC_2H_5)_4$); also referred to as TEOS in English), and a larger isolation layer 41, which is generally composed of silicon nitride Si_3N_4. Silicon nitride enables better etching of the spacers while the smaller isolation layer forms a buffer layer against the stresses induced in the underlying silicon by the nitride layer.

The manufacture of the transistor also comprises a stage wherein the source, drain and gate regions of the transistor are subjected to a silicidation process. This silicidation process includes, inter alia, the deposition of a metal, such as titanium or cobalt, which, in combination with silicon, is capable of forming a metal silicide, for example titanium silicide $TiSi_2$. This results in the formation of metal silicide zones 5, 6 and 7, which are provided on, respectively, the gate, source and drain regions of the transistor.

The silicidation stage enables a less elevated resistance of the polysilicon track 2 to be obtained.

However, as shown in Figure 1, the silicide zone 5 contacting the polysilicon region 2 has a curved interface with this polysilicon region, which is caused by mechanical stresses induced during the chemical reaction between titanium and silicon.

Apart from the fact that said curved surface is less suitable for making contact, at a later stage, than a flat surface, the thickness of the silicide formed is smaller at certain locations, and it has been found that the bonding power obtained would cause a partial retreat of the silicide during subsequent process steps. Finally, this results in a smaller quantity of silicide, causing a smaller reduction of the resistance of the polysilicon track.

It is an object of the invention to overcome this problem.

The invention more particularly aims at improving the silicidation of the polysilicon tracks, thereby causing, in particular, the adhesion of the silicide to the silicon to be improved and hence a more efficacious reduction of the resistance of these polysilicon tracks.

The invention also aims at reducing the mechanical stresses induced in the polysilicon in the course of the silicidation process, thus enabling, in particular, a substantially flat upper silicide surface to be obtained.

This object is achieved in accordance with the invention by a method of manufacturing an integrated circuit, which method includes a stage wherein lateral isolation regions (spacers) are formed at the sides of at least one projecting polysilicon region so as to be in contact therewith, said lateral isolation regions each being composed of a smaller isolation layer, which is in contact with said projecting region, and of a larger isolation layer. The method also includes a silicidation process to which the upper part of the polysilicon region is subjected, which silicidation process includes the deposition on said upper part of a metal layer which is capable of forming a metal silicide with the silicon.

In accordance with a general characteristic of the invention, the silicidation process includes, prior to the deposition of said metal layer, an etch step to which at least the vertical portion of the smaller isolation layer is subjected so as to form a trench of predetermined depth between the larger isolation layer of each lateral isolation region and the corresponding side of the polysilicon layer. Moreover, the deposition of the metal layer, for example of titanium, is a directional deposition, which is carried out using, for example, a honeycomb-structured collimator, enabling the trenches thus obtained to be correctly filled.

In other words, an etch process carried out on the smaller isolation layer (at least the vertical portion thereof) so as to detach at least the upper part of the polysilicon layer is inherent in the invention, said etch process enabling the mechanical stresses developing in this upper part during the silicidation to be reduced. In addition, filling the trenches obtained by means of the directional metal deposition results in an improved lateral silicidation of the polysilicon region. Those skilled in the art will be capable of adjusting the

desired depth of the trenches as a function of, in particular, the dimensional characteristics of the polysilicon regions and the spacers in order to achieve the effect as desired by the invention, and taking into account the intended application.

In this case, it has been found that, in order to substantially improve the silicidation, the depth of the trenches preferably should be at least $1/20^{th}$ of the height of the projecting polysilicon region.

Those skilled in the art will also be capable of adjusting the depth of the trenches in such a way that the larger isolation layer (typically of silicon nitride) of the spacers does not become detached. In this respect, it has been found that a trench depth of maximally half the height of the larger isolation layer and maximally half the thickness of the larger isolation layer would reduce the risk of said larger isolation layer becoming detached.

The vertical portion of the smaller isolation layer of the spacers may be etched using an anisotropic etch process. In this case, only the vertical portion of the smaller isolation layer of the spacers is etched.

The vertical portion of the smaller isolation layer may alternatively be etched using an isotropic etch process. This results in the formation of a horizontal trench inside each spacer, which horizontal trench is made in the smaller isolation layer between the larger isolation layer and the substrate of the integrated circuit, said horizontal trench extending from the side edge of the larger isolation layer of the spacer. Such a horizontal trench enables a further reduction of the risk of short-circuits between the silicidized source and drain regions, on the one hand, and the silicidized gate region on the other hand.

The invention also aims at providing an integrated circuit comprising lateral isolation regions formed at the sides of at least one projecting region of polysilicon so as to be in contact therewith, each lateral isolation region being composed of a smaller isolation layer, contacting said projecting region, and a larger isolation layer. The integrated circuit further comprises a zone including a metal silicide situated in the upper part of the polysilicon region.

In accordance with a general characteristic of the invention, each lateral isolation region comprises a vertical trench made in the smaller isolation layer between the larger isolation layer and the corresponding side of the projecting region, said trench extending from the top of the larger isolation layer of the corresponding lateral isolation region down to a predetermined depth.

These and other objects of the invention will be apparent from and elucidated with reference to the embodiment(s) described hereinafter.

In the drawings:

Fig 1, already described hereinabove, diagrammatically shows a transistor in accordance with the prior art, and

Figs. 2 through 8 diagrammatically show different steps in the implementation of the method in accordance with the invention; Fig. 8 more particularly shows a part of an integrated circuit in accordance with the invention.

In Fig. 2, reference numeral 1 denotes a semiconductor substrate of silicon, and reference numeral 70 denotes a lateral isolation zone, or field oxide, which is typically made of silicon dioxide, and which serves, for example, to isolate the active zone formed in the silicon substrate 1 from another active zone.

After the formation, in a customary manner, of a gate oxide layer 3, and after the deposition, in a customary manner, of a polysilicon layer and etching of the latter, polysilicon tracks 2 are obtained (shown in section in different planes), comprising, for example, a projecting region which is formed above the substrate and which serves to form the field-effect gate region of a transistor, and another projecting region which is formed above the field oxide and which serves to connect together two gate regions of two adjacent transistors.

The height of the projecting region of polysilicon 2 generally lies in the range between 1500 and 2500 Å, for example approximately 2000 Å.

Subsequently, a smaller isolation layer 400, typically of TEOS oxide, is similarly deposited in a manner which is known per se (Fig. 3), said smaller isolation layer having a thickness of the order of, for example, 200 Å. Next, a larger isolation layer 410, typically of silicon nitride, is similarly deposited in a manner which is also known per se.

After subjecting the larger isolation layer 410 to an anisotropic etch process, the configuration shown in Fig. 4 is obtained, wherein the etched, larger isolation layer 411is used to form the larger isolation layer of the spacers arranged so as to contact the vertical, lateral sides of the projecting regions of polysilicon.

It is to be noted that the smaller isolation layer 400 can be used as a stop layer in this anisotropic etch process.

Subsequently (see Fig. 5), a customary process is carried leading to a reduction of portions of the smaller isolation layer 401 obtained in Fig.4, which portions are situated on the polysilicon regions and outside the layer 411.

This results in the formation of spacers formed by the smaller isolation layer 402 and the larger isolation layer 411. The total thickness of the spacers generally lies in the

range between 50 nm and 100 nm, for example 70 nm. To be more precise, the thickness E of the larger isolation layer 411 is, for example, 50 nm while the thickness of the smaller isolation layer 402 is, for example, 20 nm.

After the customary doping operations of the drain and source regions have been carried out in the semiconductor substrate as well as the subsequent high-temperature annealing process at a temperature above, for example, 1000°C for 5 to 50 seconds, a layer 8 is deposited which is composed of a material which serves to protect a part of the integrated circuit against the subsequent silicidation step. This protection material may be silicon dioxide or TEOS oxide or TEOS oxide covered with silicon nitride.

Next (see Fig. 6), the material 8 is subjected to an etch treatment so as to remove it at the location of the region of the integrated circuit involved in the silicidation process.

If the material 8 is identical to the material used for the smaller isolation layer 402, then the etch treatment of the material 8 is extended so as to include an overetch treatment leading to the formation of a vertical trench TR having a predetermined depth h between the larger isolation region 411 of the spacers and the corresponding side F of the projecting polysilicon region.

If, however, the material 8 differs from the material of the smaller isolation layer 402 of the spacers, then an additional, selective etch treatment is carried out to form the trenches TR.

If the etch treatment of the material 8 and, possibly, the additional etch treatment are anisotropic etch treatments, then only the vertical portion of the smaller isolation layer 402 is etched. In this case, preferably, but not necessarily, one or more isotropic etch processes are carried out in order to form also horizontal trenches TH between the larger isolation layer 411 and the substrate 1, said trenches extending from the outer lateral edge of the larger isolation layer 411 of the spacers. The function and the usefulness of these horizontal trenches TH will be described hereinbelow.

The depth h of the vertical trenches TR is preferably at least equal to $1/20^{th}$ of the height H of the projecting polysilicon region, resulting in a substantial improvement of the silicidation by a reduction of the mechanical stresses in the polysilicon.

Moreover, in order to preclude that the larger isolation layer 411 of the spacers becomes detached, said depth h preferably remains below half the height H1 of the larger isolation layer 411, and also below half the thickness E of said layer 411.

This means, in a practical indication of the above ratios, that for a height H of the polysilicon of the order of 200 nm, a height h of the order of at least 10 nm leads to a substantial improvement of the silicidation.

It is to be noted that the presence of the oblique sides FO on the field oxide 70 is caused by oxide consumption during the manufacturing process.

When the trenches have been formed, a metal 9 (see Fig.7) which is capable of forming a metal silicide with the polysilicon is deposited. This is a directional deposition which is carried out using, for example, a honeycomb-structured collimator, so that the trenches TR can be filled, which would not be possible if use was made of a customary powder-coating process.

After the silicidation step, a first annealing step is carried out using equipment that is known per se, said annealing step being carried out a temperature in the range between 650°C and 800°C (for titanium) for a period of time ranging between 10 and 30 seconds, and a temperature of, for example 450°C for cobalt.

This first annealing process causes the titanium to be converted to titanium silicide $TiSi_2$, more particularly to a titanium silicide known to those skilled in the art as $TiSi_2$-C49. This formation of titanium silicide takes place through contact with the polysilicon as well as through contact with the silicon of the substrate.

Through contact with the larger isolation layer 411 of the spacers, titanium nitride TiN and titanium oxides TiO_x are formed. Titanium nitrides also form above the titanium silicide.

It is to be noted that the trenches TR, which have been filled with titanium at an earlier stage, improve the lateral silicidation of the polysilicon regions.

After the first annealing process, a selective reduction, which is known per se, of the titanium nitride, the titanium oxides TiO_x and the titanium is carried out. This selective reduction is obtained, for example, by wet-etching in a bath on the basis of ammonia and hydrogen peroxide (H_2O_2). It is to be noted that a small quantity of $TiSi_2$ is consumed in this wet-etching process.

Subsequently, a second high-temperature annealing process is carried out, typically at temperatures above 800°C, for example 900°C, for a few seconds, for example about ten seconds, in order to convert the titanium silicide C49 to a less resistive titanium silicide known to those skilled in the art as C54. Also in this case, the conversion takes place under more favorable conditions than in the method according to the prior art, which can be

attributed to the reduction of the mechanical stresses in the polysilicon, which reduction is attributable to the presence of vertical trenches.

After said annealing process, the configuration shown in Fig. 8 is obtained. In Fig. 8, reference numeral 5 denotes the metal silicide zone situated on the upper part of the projecting regions of silicon. Reference numerals 6 and 7 denote the metal silicide zones situated on the source and drain regions of the transistor. The upper surface of the metal silicide zone 5 is quasi planar. Furthermore, in the course of the annealing processes, particularly during the first annealing process, a small portion of the silicon is consumed. However, if said reduction in height is taken into account as well as the height of the metal silicide 5, a height H2 of the silicidized polysilicon region is obtained which is approximately equal to the initial height H of the polysilicon region.

Consequently, the height h of the vertical trenches TR remains preferably equal to at least $1/20^{th}$ of the height H2.

Furthermore, the selective reduction of the titanium oxides, the titanium nitride and, possibly, the unreacted titanium, carried out between the two annealing processes, may result in titanium nitride residues and/or titanium oxide residues being left behind on the surface of the larger isolation layer 411, which residues may cause short-circuits between the zones if they simultaneously contact the silicidized gate zones and the silicidized drain/source zones. This risk of short-circuits is minimized by the presence of the horizontal trenches TH

CLAIMS:

1. A method of manufacturing an integrated circuit, which method includes a stage wherein lateral isolation regions (spacers) are formed at the sides of a projecting polysilicon region so as to be in contact therewith, said lateral isolation regions each being composed of a smaller isolation layer (402), which is in contact with said projecting region (2), and of a larger isolation layer, which method also includes a silicidation process to which the upper part of the polysilicon region is subjected, which silicidation process includes the deposition on said upper part of a metal layer which is capable of forming a metal silicide (5) with the silicon, characterized in that the silicidation process includes, prior to the deposition of said metal layer, an etch step to which at least the vertical portion of the smaller isolation layer (402) is subjected so as to form a trench (TR) of predetermined depth (h) between the larger isolation layer (411) of each lateral isolation region and the corresponding side (F) of the polysilicon region (2), and in that the deposition of the metal layer is a directional deposition.

2. A method as claimed in claim 1, characterized in that the depth (h) of the trench is at least equal to $1/20^{th}$ of the height (H) of the projecting region.

3. A method as claimed in claim 1 or 2, characterized in that the depth (h) of the trench is equal to maximally half the height (H1) of the larger isolation layer and maximally half the thickness (E) of the larger isolation layer.

4. A method as claimed in any one of the preceding claims, characterized in that the vertical portion of the smaller isolation layer (402) is anisotropically etched.

5. A method as claimed in any one of the claims 1 to 3, characterized in that the vertical portion of the smaller isolation layer (402) is isotropically etched.

6. An integrated circuit comprising lateral isolation regions formed at the sides of at least one projecting region of polysilicon so as to be in contact therewith, each lateral

isolation region being composed of a smaller isolation layer (402), contacting said projecting region (2), and a larger isolation layer (411), and comprising a zone (5) including a metal silicide situated in the upper part of the polysilicon region (2), characterized in that each lateral isolation region comprises a vertical trench (TR) made in the smaller isolation layer (402) between the larger isolation layer (411) and the corresponding side (F) of the projecting region (2), said trench (TR) extending from the top of the larger isolation layer (411) of the corresponding lateral isolation region down to a predetermined depth (h).

7. An integrated circuit as claimed in claim 6, characterized in that the depth (h) of the trench (TR) is at least equal to $1/20^{th}$ of the height (H2) of the projecting region of silicidized polysilicon.

8. An integrated circuit as claimed in claim 6 or 7, characterized in that the depth (h) of the trench (TR) is equal to maximally half the height (H1) of the larger isolation layer and equal to maximally half the thickness(E) of the larger isolation layer.

9. An integrated circuit as claimed in any one of the claims 6 to 8, characterized in that each lateral isolation region comprises a horizontal trench (TH) made in the smaller isolation layer (402) between the larger isolation layer (411) and the substrate (1) of the integrated circuit, said trench extending from the lateral edge of the larger isolation layer of the lateral isolation region.

ABSTRACT:

The integrated circuit comprises lateral isolation regions formed at the sides of at least one projecting polysilicon region so as to be in contact therewith, said lateral isolation regions each being composed of a smaller isolation layer (402), which is in contact with said projecting region (2), and of a larger isolation layer (411), and it further comprises a zone (5) including a metal silicide situated in the upper part of the polysilicon region (2). Each lateral isolation region comprises a vertical trench (TR) made in the smaller isolation layer (402) between the larger isolation layer (411) and the corresponding side (F) of the projecting region (2), said trench (TR) extending from the top of the larger isolation layer (411) of the corresponding lateral isolation region down to a predetermined depth (h).

Figure 8.

FIG.1

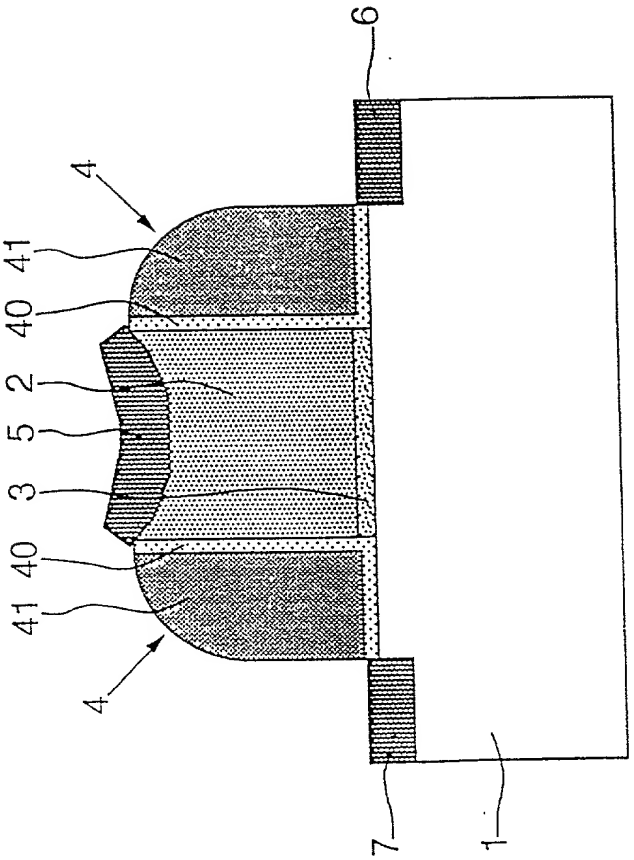


FIG.2

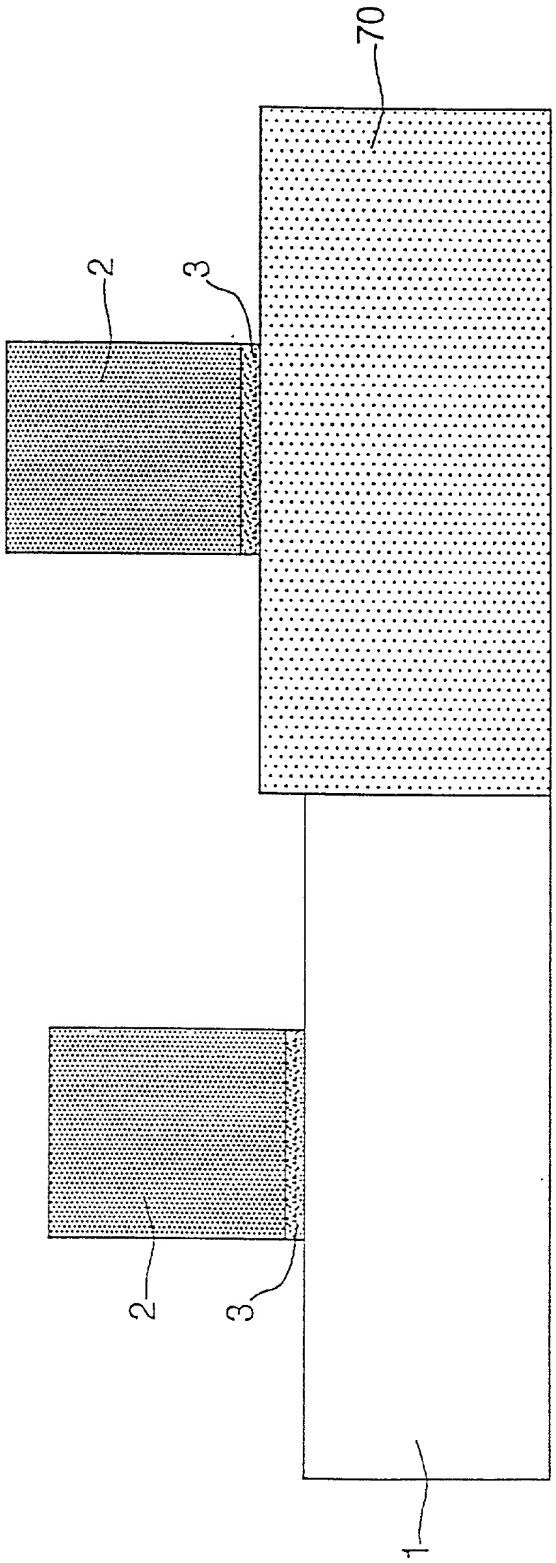


FIG.3

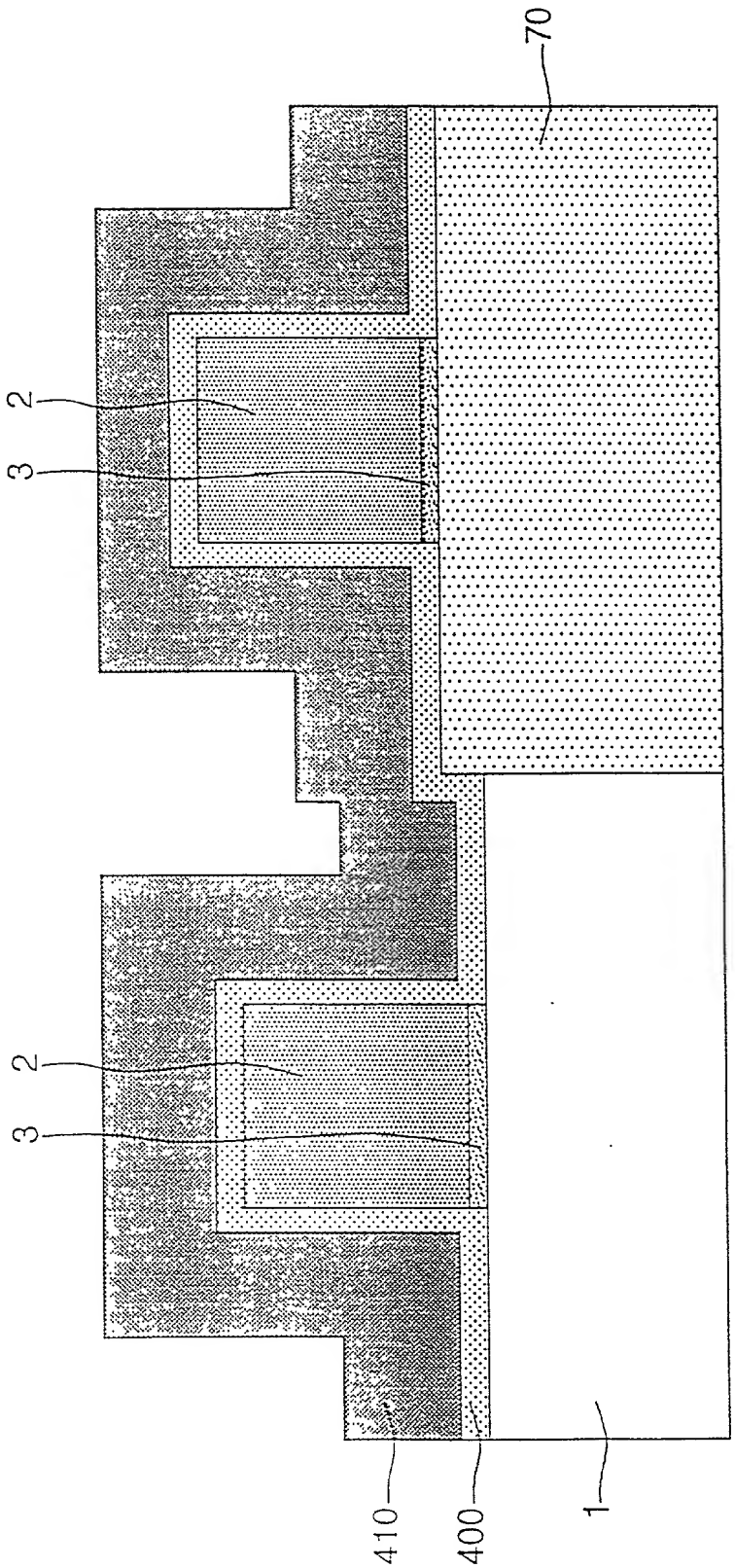


FIG.4

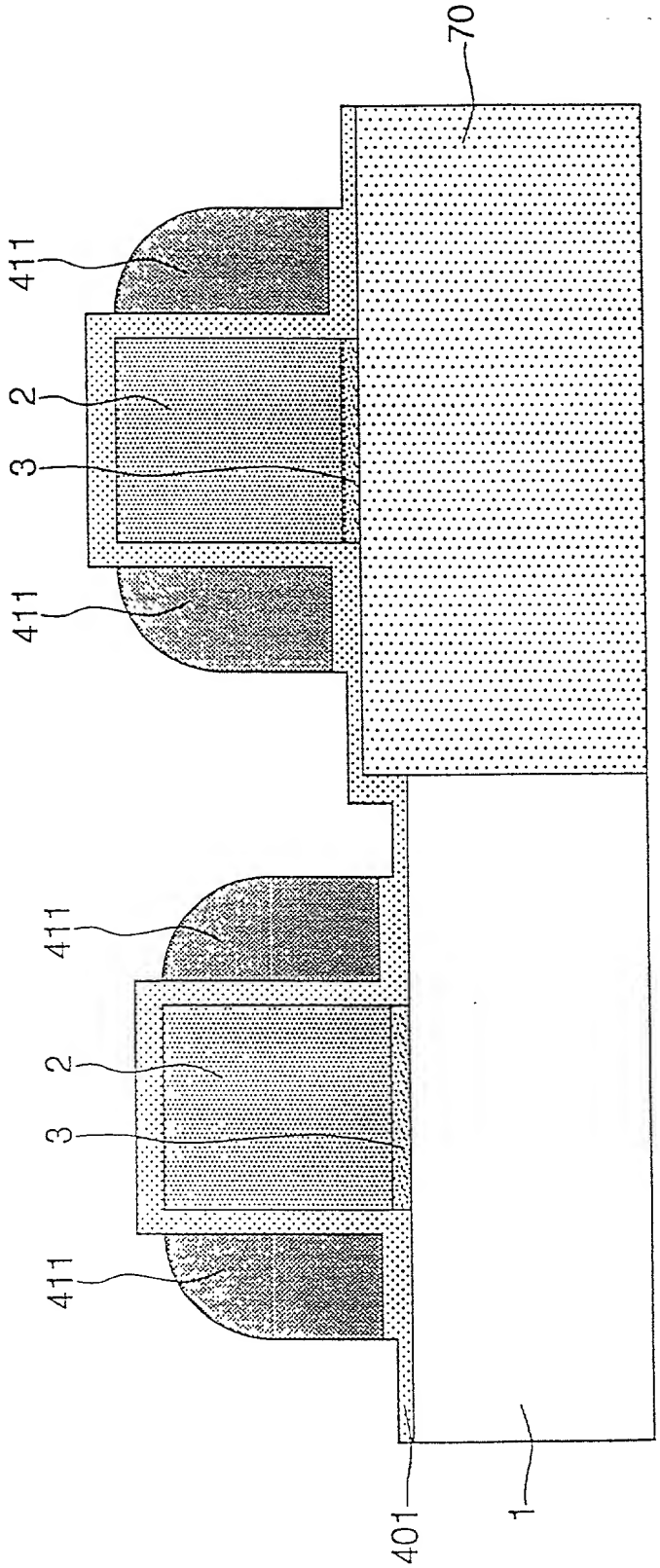


FIG.5

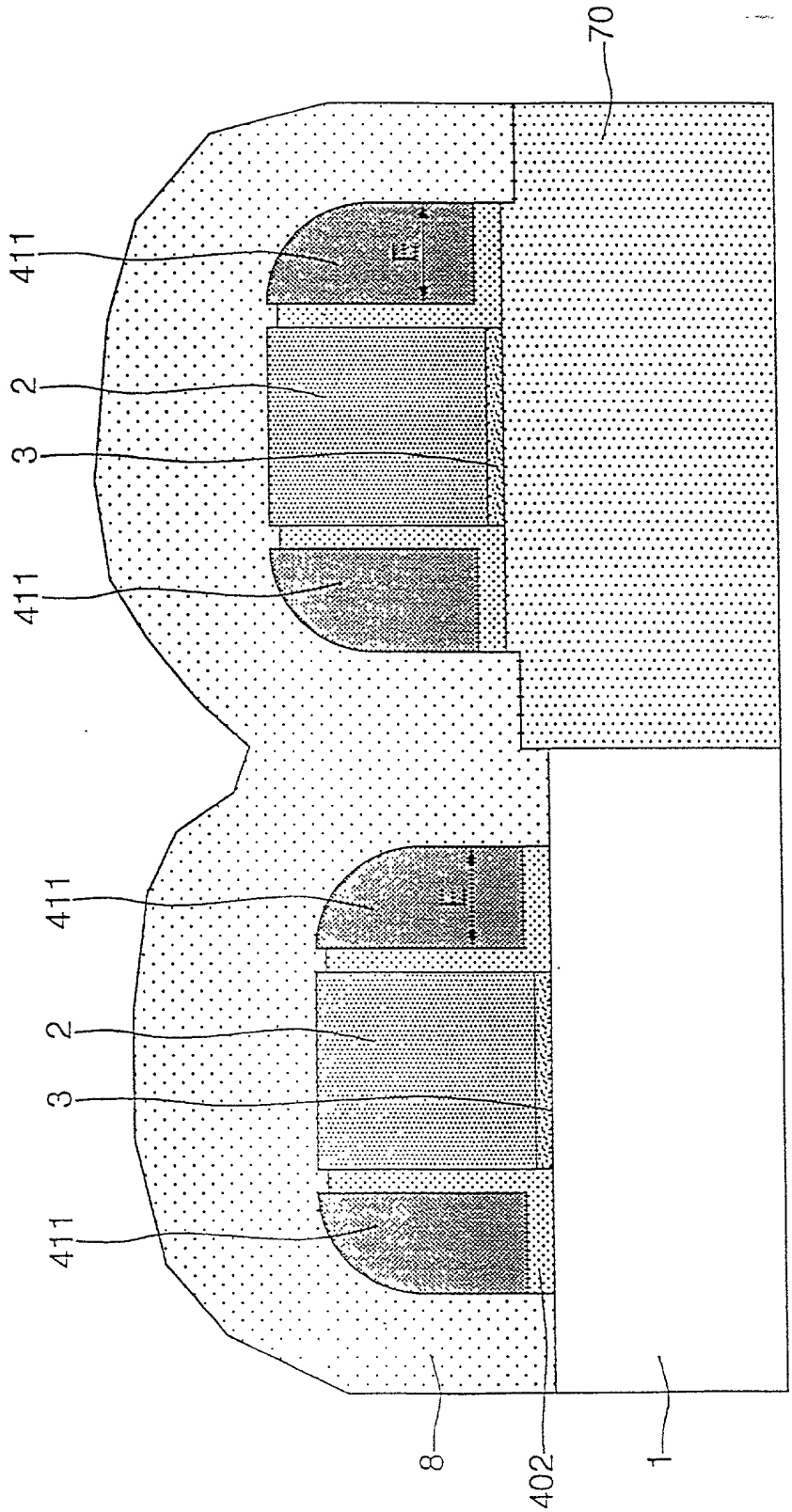


FIG.6

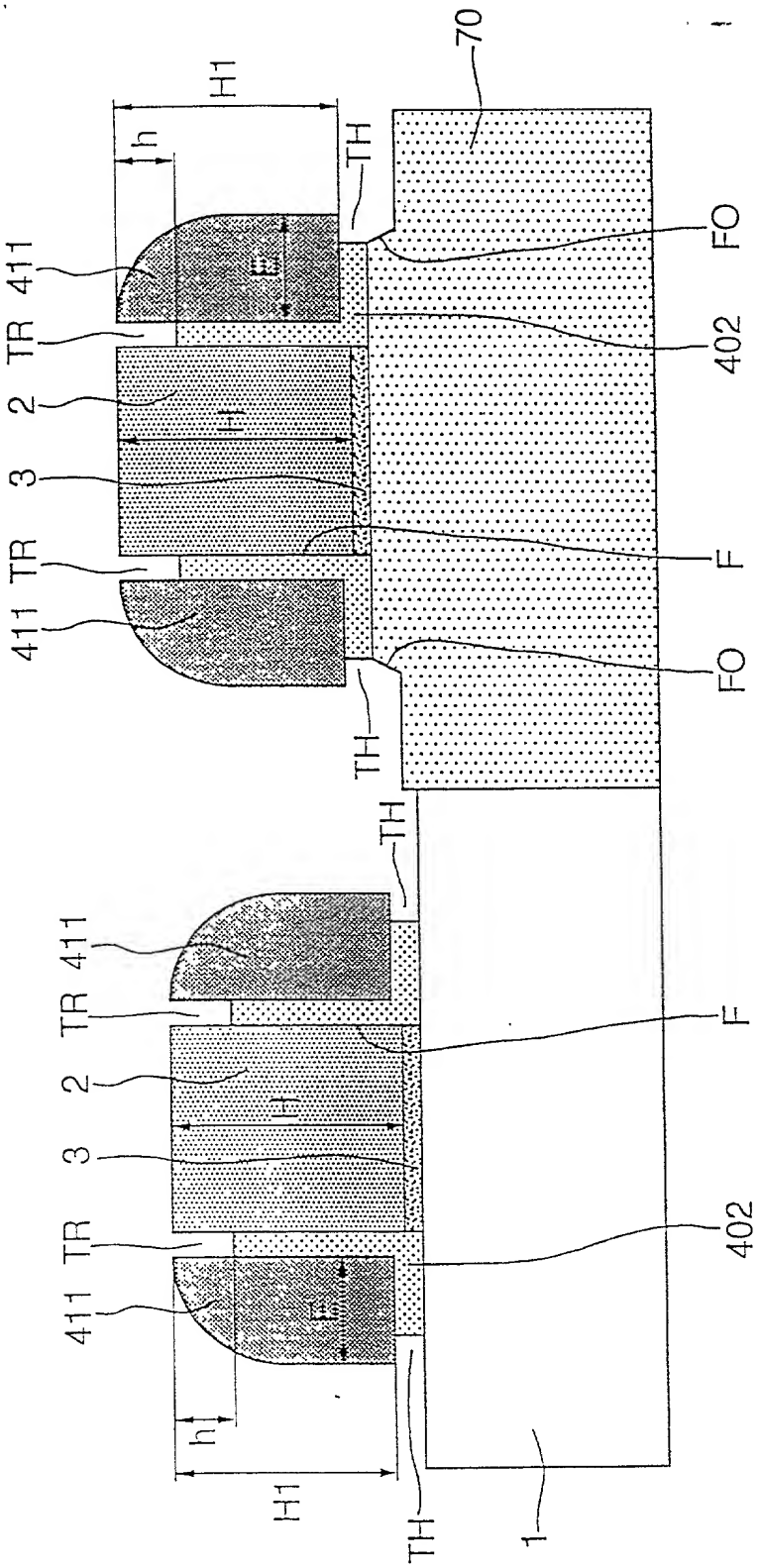


FIG.7

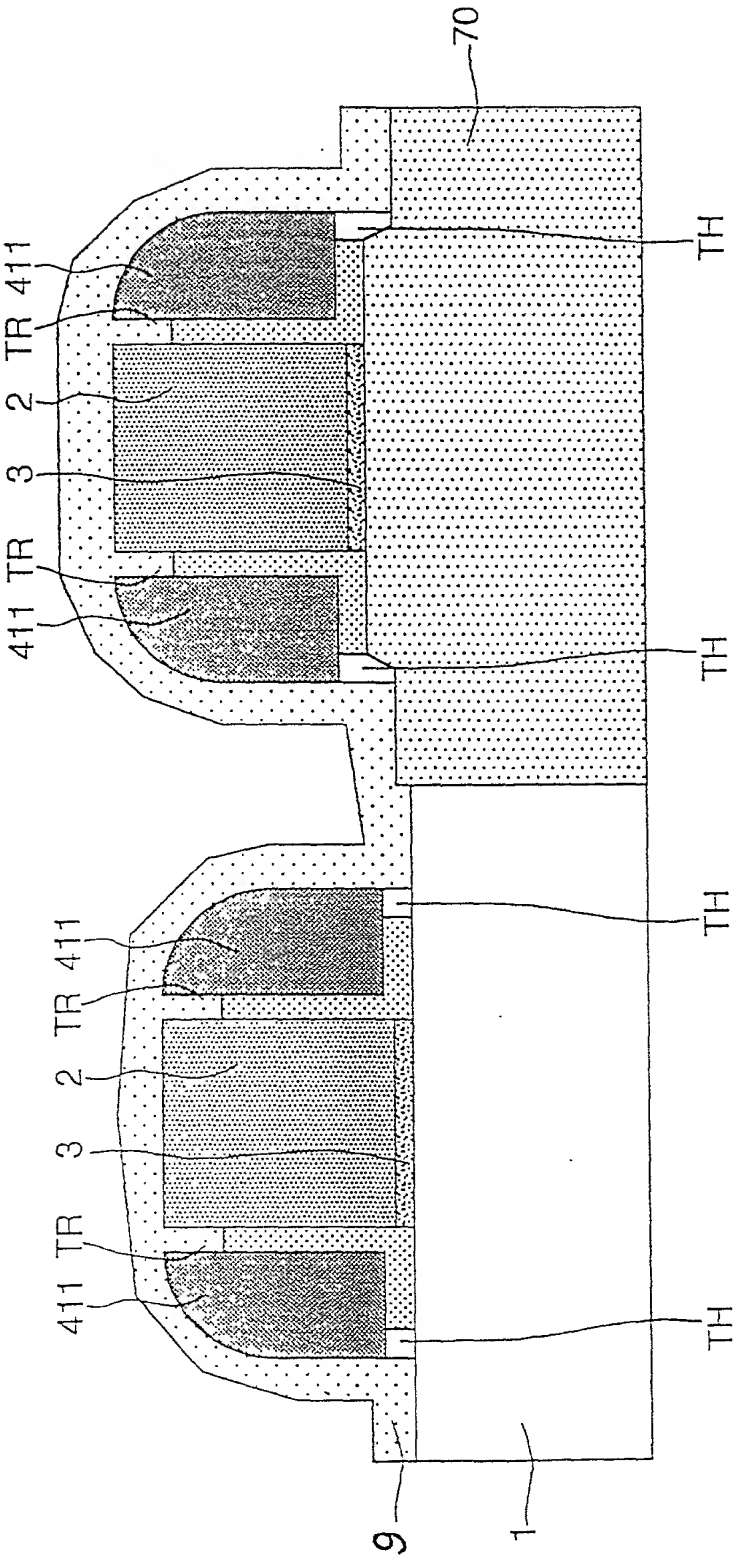
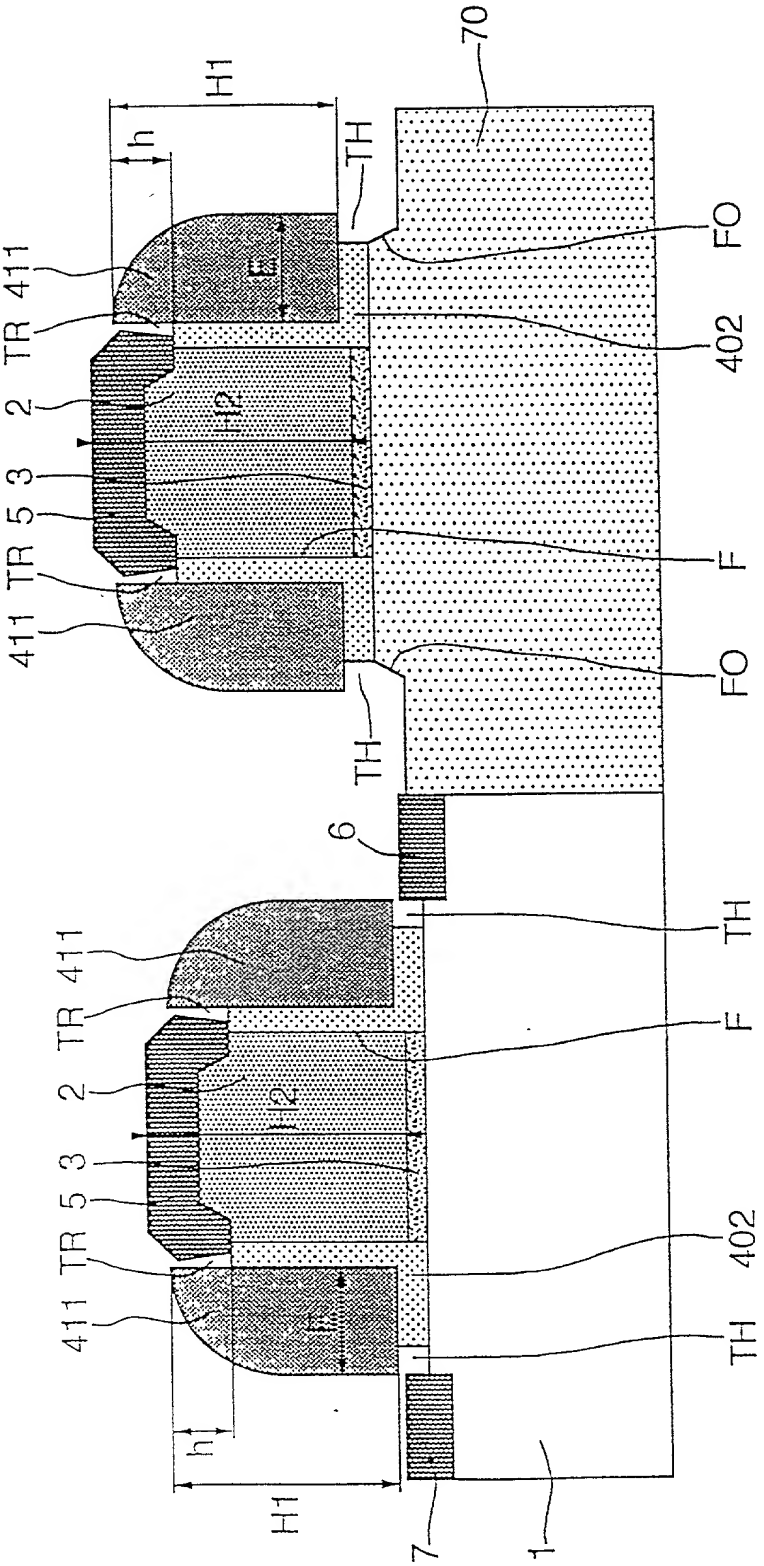


FIG.8



COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY (includes Reference to PCT International Applications)	ATTORNEY'S DOCKET NUMBER **PHQ 99.010 US**

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **"Method of manufacturing an integrated circuit comprising an improved silicidation and a coresponding integrated circuit"**
the specification of which (check only one item below):

☐ is attached hereto.

☐ was filed as United States application

Serial No _____

on _____

and was amended

on _____

☒ was filed as PCT international application

Number PCT/EP00/07519

on 2 August 2000

and was amended under PCT Article 19

on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

PRIOR FOREIGN/PCT APPLICATION(S) AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. 119:

COUNTRY	APPLICATION NUMBER	DATE OF FILING DAY, MONTH, YEAR	PRIORITY CLAIMED UNDER 35 USC 119
France	**9910309**	**09 August 1999**	**YES**

Combined Declaration For Patent Application and Power of Attorney (Continued) (includes Reference to PCT International Applications)	Attorneys Docket Number **PHQ 99.010 US**

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) abnd/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (List name and registration number)

Algy Tamoshunas Reg. No. 27,677 Jack E. Haken, Reg. No. 26,902	Direct Telephone Calls to: (name and telephone number) (914)332-0222

201	FULL NAME OF INVENTOR	FAMILY NAME **DE COSTER**	FIRST GIVEN NAME **Walter**	SECOND GIVEN NAME **Jan August**
	RESIDENCE & CITIZENSHIP	CITY **Diepenbeek**	STATE OR FOREIGN COUNTRY **Belgium** BEX	COUNTRY OF CITIZENSHIP **Belgium**
	POST OFFICE ADDRESS	POST OFFICE ADDRESS **Kapelstraat 56**	CITY **B-3590 Diepenbeek**	STATE & ZIP CODE/COUNTRY **Belgium**
202	FULL NAME OF INVENTOR	FAMILY NAME **GERRITSEN**	FIRST GIVEN NAME **Eric**	SECOND GIVEN NAME
	RESIDENCE & CITIZENSHIP	CITY **Nijmegen**	STATE OR FOREIGN COUNTRY **The Netherlands** NLX	COUNTRY OF CITIZENSHIP **The Netherlands**
	POST OFFICE ADDRESS	POST OFFICE ADDRESS **Heliodoorstraat 5**	CITY **6534 SH Nijmegen**	STATE & ZIP CODE/COUNTRY **The Netherlands**
203	FULL NAME OF INVENTOR	FAMILY NAME **BASSO**	FIRST GIVEN NAME **Marie-Therese**	SECOND GIVEN NAME
	RESIDENCE & CITIZENSHIP	CITY **Meylan**	STATE OR FOREIGN COUNTRY **France**	COUNTRY OF CITIZENSHIP **France**
	POST OFFICE ADDRESS	POST OFFICE ADDRESS **38, Chemin de la Taillat**	CITY **F-38240 Meylan**	STATE & ZIP CODE/COUNTRY **France**
204	FULL NAME OF INVENTOR	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME
	RESIDENCE & CITIZENSHIP	CITY	STATE OR FOREIGN COUNTRY	COUNTRY OF CITIZENSHIP
	POST OFFICE ADDRESS	POST OFFICE ADDRESS	CITY	STATE & ZIP CODE/COUNTRY
205	FULL NAME OF INVENTOR	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME
	RESIDENCE & CITIZENSHIP	CITY	STATE OR FOREIGN COUNTRY	COUNTRY OF CITIZENSHIP
	POST OFFICE ADDRESS	POST OFFICE ADDRESS	CITY	STATE & ZIP CODE/COUNTRY

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true: and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 if Title 18 of the United states Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

SIGNATURE OF INVENTOR 201 CITY	SIGNATURE OF INVENTOR 202	SIGNATURE OF INVENTOR 203
DATE 1 March 2001	DATE 1 March 2001	DATE
SIGNATURE OF INVENTOR 204	SIGNATURE OF INVENTOR 205	
DATE	DATE	

COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY (includes Reference to PCT International Applications)	ATTORNEY'S DOCKET NUMBER **PHQ 99.010 US**

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	RESIDENCE & CITIZENSHIP	CITY	STATE OR FOREIGN COUNTRY	COUNTRY OF CITIZENSHIP
	POST OFFICE ADDRESS	POST OFFICE ADDRESS	CITY	STATE & ZIP CODE/COUNTRY

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SIGNATURE OF INVENTOR 201 CITY	SIGNATURE OF INVENTOR 202	SIGNATURE OF INVENTOR 203 Marie-Thérèse Basso
DATE	DATE	DATE 1 March 2001
SIGNATURE OF INVENTOR 204	SIGNATURE OF INVENTOR 205	
DATE	DATE	

United States Patent & Trademark Office

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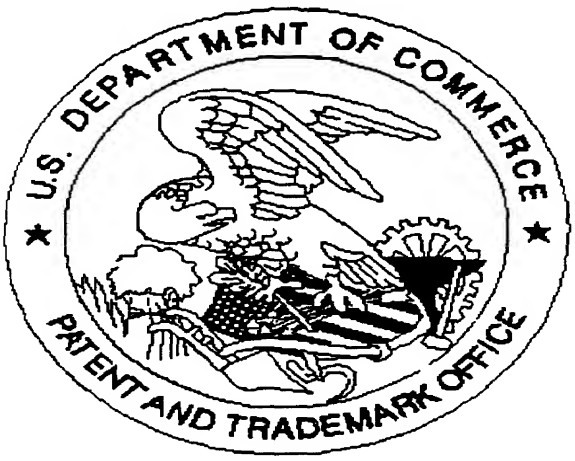

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Appendix is page 4 of The Preliminary Amendment.

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